2014 DISCOVERY SUMMIT
EXPLORING DATA INSPIRING INNOVATION

High-Speed Hardware Interface Development With Design of Experiments

Richard Allred & Barry Katz, SiSoft

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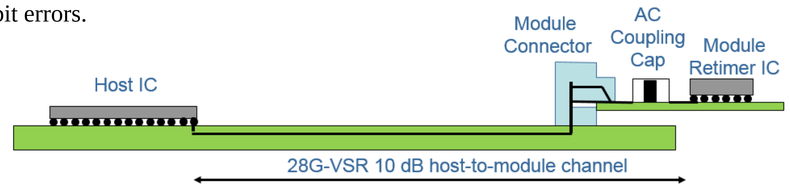
Abstract

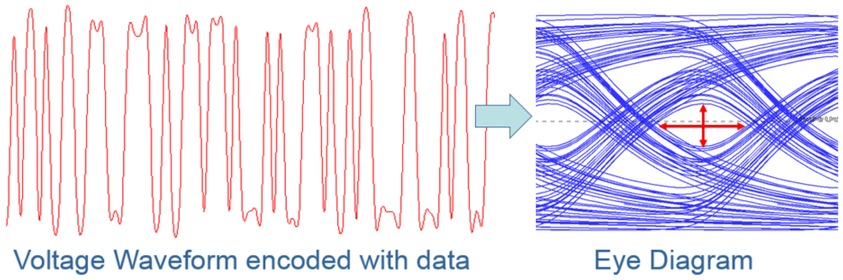
- The explosive growth of internet usage brings with it a huge demand in bandwidth capabilities. This has forced the computer communication industry to continually push the limits to improve line speed, density and power consumption of communication links.
- The design of these links is a highly complex task, where multiple objectives such as cost, performance and power must be weighed to create a competitive product. This poster describes and demonstrates how the Design of Experiments and Response Surface Modeling techniques were used to answer design problems, to quantify manufacturing variation and estimate Yield performance. This effort resulted in the industry's first 100 Gigabit Ethernet CMOS PHY chipset.

Objective

- Design a high speed 28G-VSR computer interface or link with a low probability of bit errors.

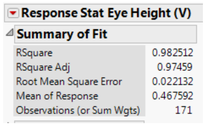


- A data rate of 28 Giga-bits per second (Gbps) means that the receiver of the link has only ~35 ps to decide if a 1 or 0 was sent.
- One measure of the goodness of a link is the voltage eye diagram inner height and width. The lower spec limit for eye height and width is 200 mV and 20 ps respectively. Additionally a PPM limit of 1000 is desired.



Method

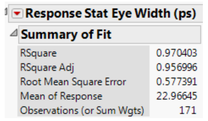
- We utilized SiSoft's advanced computer interface simulation techniques to virtually construct and test many different configurations.
- Utilizing past experience, 9 factors were selected to explore the space: 3 design factors and 6 manufacturing factors (uncontrolled). Factor Details.
- Most of the factors are discrete and a full factorial design required 26,244 simulations which would take **58 hours** of compute time.
- A D-Optimal RSM model with 171 runs (3 times the minimum) were used to sample the factor space. This required only **20 minutes** of compute time.
- A RSM model was used which yielded excellent fits on the eye height and width.



Response Stat Eye Height (V)

Summary of Fit

RSquare	0.982512
RSquare Adj	0.97459
Root Mean Square Error	0.022132
Mean of Response	0.467592
Observations (or Sum Wgts)	171



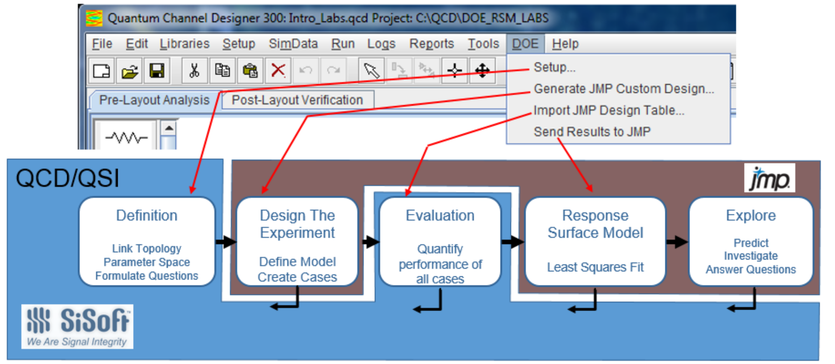
Response Stat Eye Width (ps)

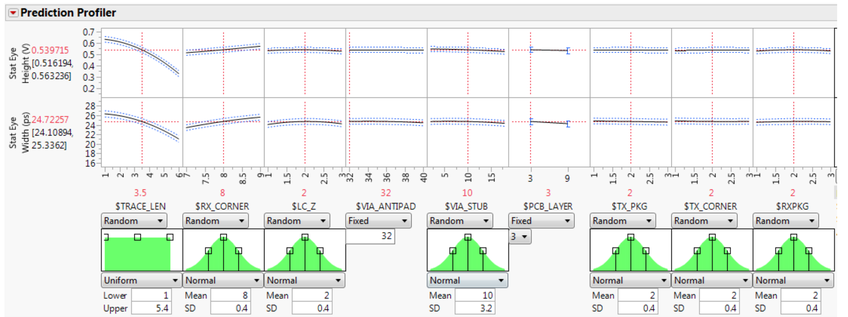
Summary of Fit

RSquare	0.970403
RSquare Adj	0.956996
Root Mean Square Error	0.577391
Mean of Response	22.96645
Observations (or Sum Wgts)	171

Results

- The Prediction Profiler was used to predict the worst case operating conditions. Two of the design factors (printed circuit board (PCB) layer and via anti-pad size) were used to improve the worst case performance.
- The Simulator was utilized to assign distributions to the manufacturing factors and to quantify the probability of the worst case condition occurring through PPM analysis.
- The upper limit of the PCB trace length, the most signification of the factors and the last design factor, was reduced to 5.4 inches which yielded a PPM of around 1087.



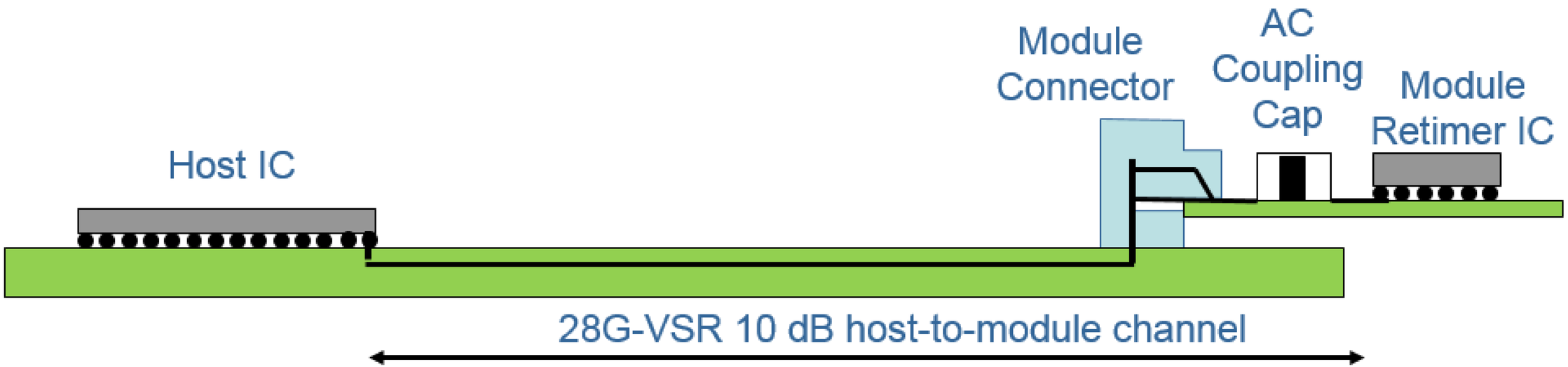


Conclusions

- It has been demonstrated that the design of a challenging state of the art computer system can be greatly enhance by utilizing Design of Experiments and response surface modeling. Alternative methods of design space exploration require many more manual decisions which can often lead to sub-optimal results.
- Utilizing this methodology, the round trip analysis from the design of the experiment to the analysis typically takes only minutes. This allows for the designer to quickly iterate designs to balance trade-offs and inform design decisions. SiSoft has worked closely with JMP to integrate the tools to allows for this analysis.

About the Authors

28G VSR Channel Diagram



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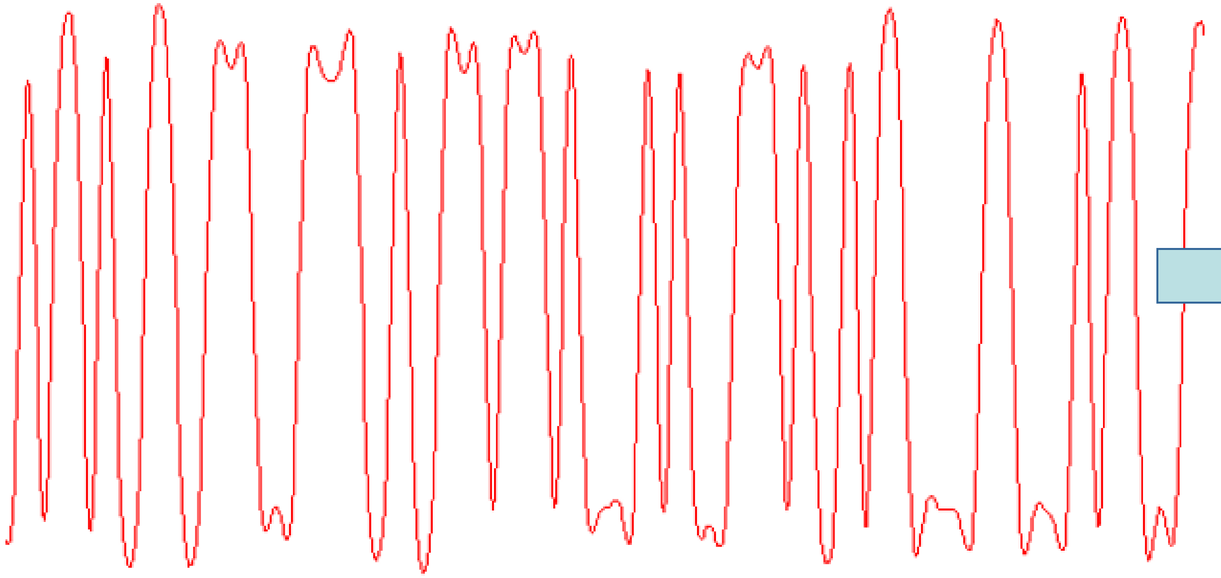
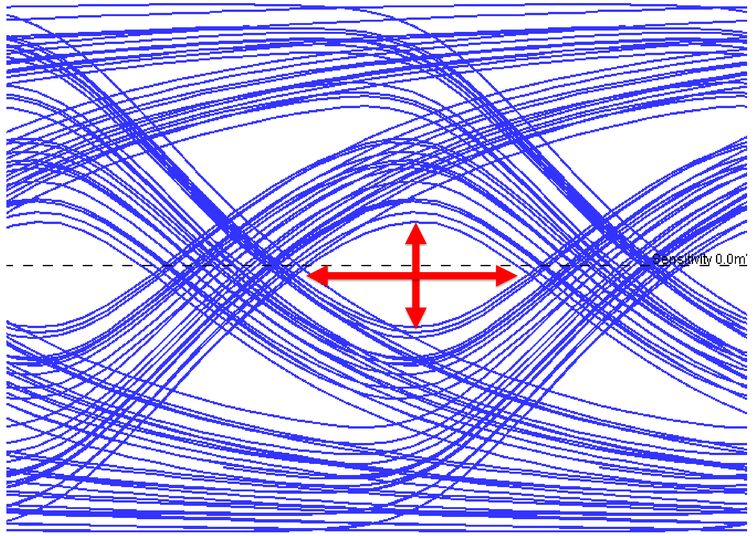
Eye Diagram



Voltage Waveform encoded with data



Eye Diagram

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Factor Details

Parameter Name	Factor Type	Min	Typ	Max
Tx PVT Corner	Manufacturing	SS	TT	FF
Tx PKG	Manufacturing	90 Ohm	100 Ohm	110 Ohm
Line Card PCB Via Anti-Pad Size	Design	32 mil	36 mil	40 mil
Line Card PCB Via Stub length	Manufacturing	2 mil	10 mil	18 mil
Line Card PCB Routing Layer	Design	3	--	9
Line Card length	Design	1 inch	3 inch	6 inch
Line Card TL Impedance	Manufacturing	90 Ohm	100 Ohm	110 Ohm
Rx PKG	Manufacturing	90 Ohm	100 Ohm	110 Ohm
Rx PVT Corner	Manufacturing	SS	TT	FF

Table 1: 28G VSR interface factor space definition.

- Full factorial design requires 26,244 simulations which would take **58 hours** of compute time.

- A D-Optimal RSM model with 171 runs (3 times the minimum) were used to sample the factor space. This required only **20 minutes** of compute time.

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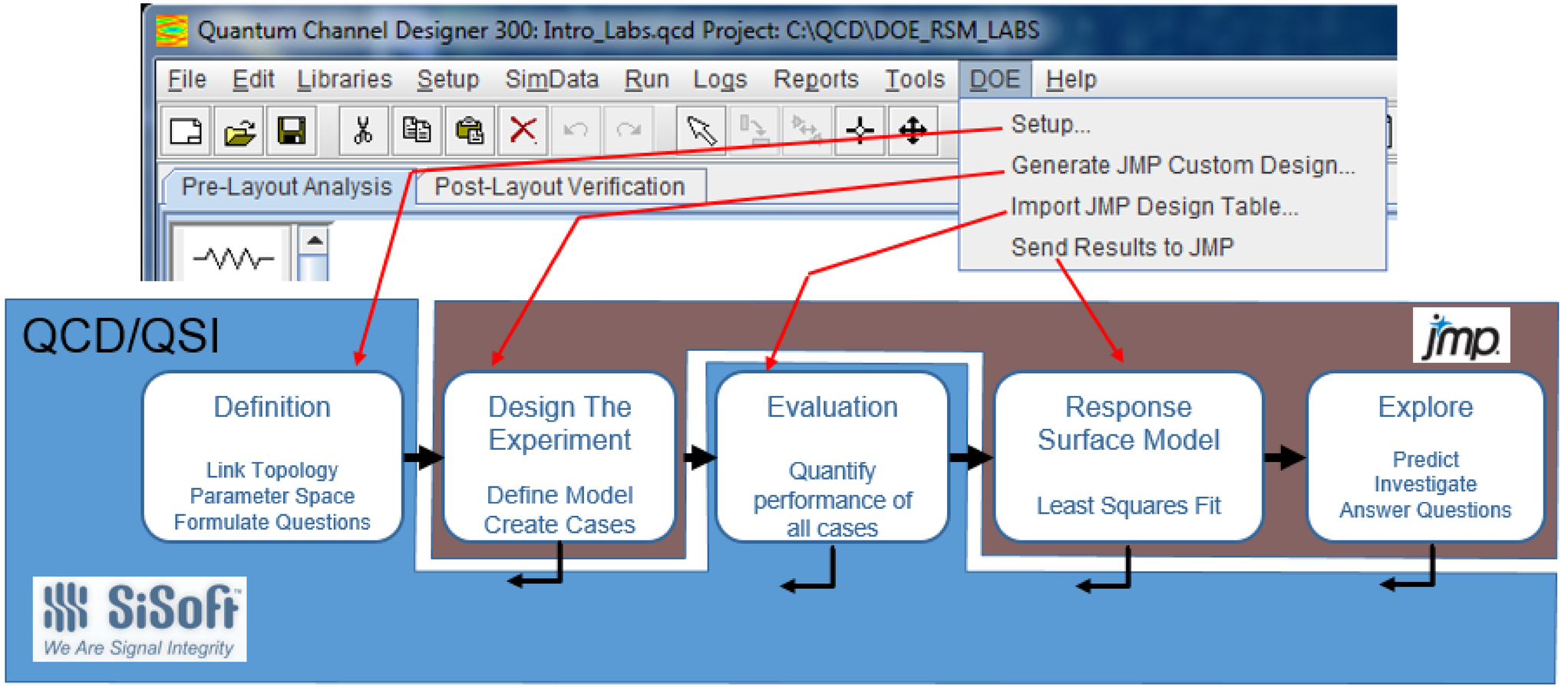
JMP/SiSoft Analysis Flow



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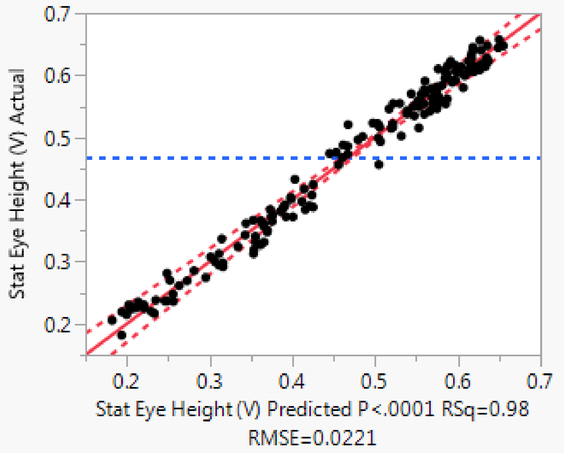
Model Fit Summary

Response Stat Eye Height (V)

Actual by Predicted Plot



Summary of Fit

RSquare	0.982512
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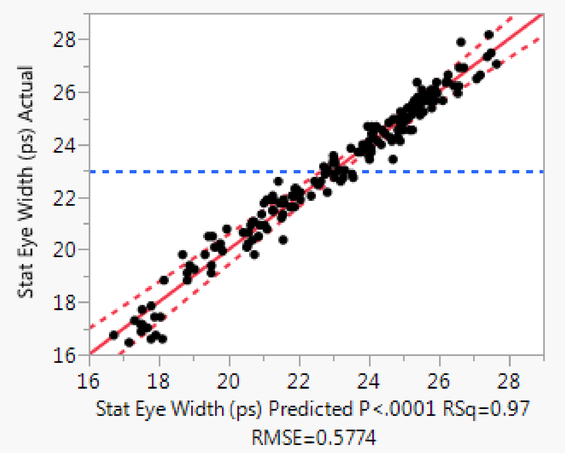
Analysis of Variance

Source	DF	Sum of Squares	Mean Square	F Ratio
Model	53	3.2197294	0.060750	124.0224
Error	117	0.0573098	0.000490	Prob > F
C. Total	170	3.2770392		<.0001*

Response Stat Eye Width (ps)

Actual by Predicted Plot



Summary of Fit

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Mean of Response	22.96645
Observations (or Sum Wgts)	171

Analysis of Variance

Source	DF	Sum of Squares	Mean Square	F Ratio
Model	53	1278.8743	24.1297	72.3789
Error	117	39.0055	0.3334	Prob > F
C. Total	170	1317.8798		<.0001*

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Analysis Details

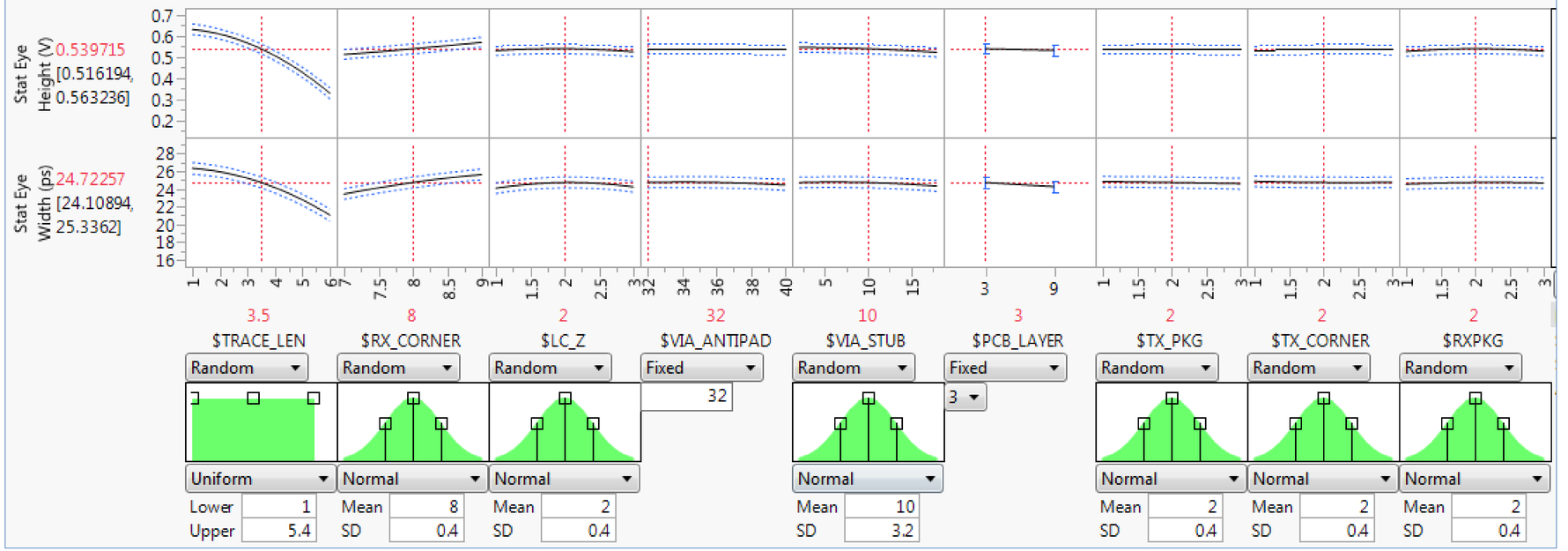
Variable Importance: Independent Uniform Inputs

Summary Report

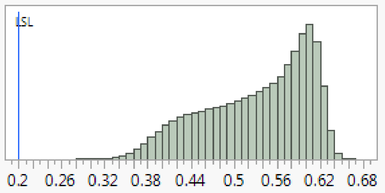
Overall

Column	Main Effect	Total Effect
$TRACE_LEN	0.518	0.584
$RX_CORNER	0.056	0.061
$LC_Z	0.018	0.018
$VIA_ANTIPAD	0.015	0.015
$VIA_STUB	0.014	0.014
$PCB_LAYER	0.012	0.012
$TX_PKG	0.011	0.011
$TX_CORNER	0.011	0.011
$RXPKG	0.01	0.01

Prediction Profiler



Stat Eye Height (V)



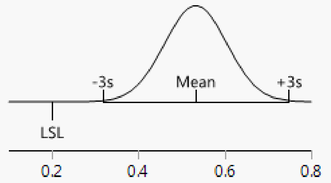
Spec Limits

Response	LSL	USL
Stat Eye Height (V)	0.2	.
Stat Eye Width (ps)	20	.

Capability Analysis

Specification	Value	Portion	% Actual
Lower Spec Limit	0.2	Below LSL	0.0000
Spec Target	.	Above USL	.
Upper Spec Limit	.	Total Outside	0.0000

Long Term Sigma

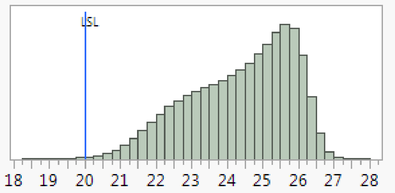


Sigma = 0.07194

Capability	Index	Lower CI	Upper CI
CP	.	.	.
CPK	1.542	1.540	1.544
CPM	.	.	.
CPL	1.542	1.540	1.544
CPU	.	.	.

Portion	Percent	PPM	Sigma Quality
Below LSL	0.0002	1.8668	6.126
Above USL	.	.	.
Total Outside	0.0002	1.8668	6.126

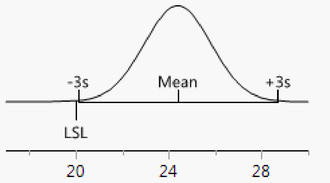
Stat Eye Width (ps)



Capability Analysis

Specification	Value	Portion	% Actual
Lower Spec Limit	20	Below LSL	0.0760
Spec Target	.	Above USL	.
Upper Spec Limit	.	Total Outside	0.0760

Long Term Sigma



Sigma = 1.43168

Capability	Index	Lower CI	Upper CI
CP	.	.	.
CPK	1.022	1.020	1.023
CPM	.	.	.
CPL	1.022	1.020	1.023
CPU	.	.	.

Portion	Percent	PPM	Sigma Quality
Below LSL	0.1088	1087.8744	4.565
Above USL	.	.	.
Total Outside	0.1088	1087.8744	4.565

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About the Authors

- **Richard Allred** is a Senior Member of Technical Staff at SiSoft where he is responsible for the modeling the industry's cutting edge transmitter and receivers and well as contributes to tool and analysis development. Previously, Richard worked at Inphi and Intel where he designed serial and parallel computer interfaces for high end applications. Richard received his MSEE from University of Utah, and has 5 publications.

- **Barry Katz**, President and CTO for SiSoft, founded SiSoft in 1995. As CTO, Barry is responsible for leading the definition and development of SiSoft's products. He has devoted much of his efforts at SiSoft to delivering a comprehensive design methodology, software tools, and expert consulting to solve the problems faced by designers of leading edge high-speed systems. He was the founding chairman of the IBIS Quality committee. Barry received an MSEE degree from Carnegie Mellon and a BSEE degree from the University of Florida.

www.sisoft.com

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- Hall, S. & Heck H. (2009). Advanced Signal Integrity for High-Speed Digital Designs.
- Goos, P. & Jones, B. (2011). Optimal Design of Experiments: A Case Study Approach.

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